



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,139	09/08/2003	Tomoharu Tanaka	001701.00676	8661
22907	7590	06/01/2004		
BANNER & WITCOFF 1001 G STREET N W SUITE 1100 WASHINGTON, DC 20001			EXAMINER LE, VU ANH	
			ART UNIT 2824	PAPER NUMBER

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application N .

10/656,139

Applicant(s)

TANAKA ET AL.

Examiner

Vu A. Le

Art Unit

2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 08 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 32-41 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 32-41 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☒ Certified copies of the priority documents have been received in Application No. 10/051,372.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 01/22/02.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

The cancellation of claims 1-31 in a Preliminary Amendment filed on 09/08/03 has been made of record.

#### ***Information Disclosure Statement***

1. The information disclosure statement filed 04/19/04 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because there is no English translation of two attachments 1-2 (Korean Patents). It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609

¶ C(1).

#### ***Specification***

1. The disclosure is objected to because of the following informalities: in page 31, line 4, "date" should be changed into "data".

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

The terminology "said write control voltage" in claims 32 and 36 lack a proper antecedent basis.

The terminology "the write voltage" in claims 33 and 36 also lack a proper antecedent basis.

It is not clear if "the write voltage" in claim 33 is different from "said write control voltage" in claim 32.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 32-33 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Endoh et al (6,014,330).

Art Unit: 2824

5. With respect to claims 32-33, Endoh et al (Figures 20-27 and see col.23) describe a non-volatile semiconductor memory device comprising: a non-volatile memory cell (Fig.19); and a write circuit (23-26 and 28 in Fig.8), configured to write data in said memory cell, thereby causing an alteration in a write state of said memory cell, for changing the supply of a write control voltage ( $V_{cg}$ , Fig.10A) in order to slow down the alteration, and for terminating the alteration amid slowing down the alteration, wherein the write voltage is stepwise increased (Fig.20),
6. With respect to claim 36, Endoh et al (col.19) teach a bit line is coupled to the memory cell at its drain electrode (inherent) to which the write control voltage is applied (bit line voltage is changed in according to writing data, line 45-51, col.19).
7. With respect to claim 37, Endoh et al disclose his invention can be used in multi-bit memory device (col.30, lines 10-12)
8. Claims 32-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Sakamoto.

Sakamoto (Figures 2-3, and 15-18) disclose a non-volatile memory device comprising a multivalued memory cell and a write circuit for writing data to memory cell by increasing the gate voltage in stepwise manner (Figs.2-3) and continues the writing to next level after the first level is achieved (Fig.15)

**Conclusion**

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
10. Kawahara et al (6,134,148) disclose a semiconductor integrated circuit and data processing system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vu A. Le whose telephone number is (571)272-1871. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571)-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Application/Control Number: 10/656,139

Art Unit: 2824

Page 6

A handwritten signature in black ink, appearing to read 'Vu A. Le', written in a cursive style.

Vu A. Le  
Primary Examiner  
Art Unit 2824

05/31/04